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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,277	08/24/2001	Paul Jeffrey Garnett	5681-02700	2593

7590 12/03/2004

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EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,277	GARNETT ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-21 are presented for examination. This office action is in response to the RCE filed on 9/7/04.

Specification

2. Applicants are requested to include the status of the related U.S. applications, patents, and foreign application (i.e. GB 2369692, US 6223230, WO 99/66410, etc.) in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification.

Claim Rejections - 35 USC § 112

3. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It appears added new limitation "operable to respond to a fault state by the controlling the copying of the dirtied blocks of the main memory" was not described in the specification at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Rowlinson et al. (Rowlinson) WO 99/66402 or 35 U.S.C. 102(b) as being anticipated by Garnet U.S. Patent No. 5,991,900.

As to claim 1, *Rowlinson* discloses the invention as claimed. Rowlinson discloses a computer system comprising at least two processing sets (Fig. 1), each of processing set including a main memory (Fig. 4), and a bridge (Fig. 1 Ref. 12) connecting the processing sets, wherein at least a first processing set further includes a dirty memory (abstract) having dirty indicators for indicating dirtied blocks of the main memory of the first processing set (abstract), and wherein the bridge (Fig. 1 Ref, 12 and page 23 middle) includes a direct memory access controller (page 20 bottom, specifically "the operation of the bridge for direct memory access" reads on this limitation) that is operable to respond to a fault state (page 24 lines 5-10, "determined less than the predetermined number of bits" and Fig. 28 Ref S44) by the controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set (abstract and page 23 middle & page 24 lines 5-10).

Alternatively, Garnet discloses a computer system comprising at least two processing sets (Fig. 1), each processing set including a main memory (Fig. 4), and a bridge (Fig. 1 Ref. 12) connecting the processing sets, wherein at least a first processing set further includes a dirty memory (col. 22 lines 35-48) having dirty indicators for indicating dirtied blocks of the main memory of the first processing set, and wherein the bridge (Fig. 1 Ref, 12 and col. 22 lines 35-49) includes a direct memory access controller (col. 19 lines 37-50 specifically "the operation of the bridge for direct memory access" reads on this limitation) that is operable to respond to a fault state (col. 23 lines 9-11, "determined less than the predetermined number of bits" and Fig. 28 Ref S44) by the controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set (col. 23 lines 12-16).

As to claim 12, the claim 12 encompasses the same scope of the invention as that of the claim 1. Therefore, the claim 12 is rejected for the same reason as the claim 1.

As to claims 2 and 13, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the direct memory access controller is operable to search the dirty memory for dirty indicators indicative of dirtied blocks (col. 22 line 18 thru col. 23 line 29).

As to claims 3 and 14, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the dirty memory comprises control logic operable to search the dirty memory for dirty indicators indicative of dirtied blocks (col. 22 line 18 thru col. 23 line 29).

As to claims 4 and 15, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the control logic is operable to output references to the dirtied blocks of the main memory to be copied (col. 22 line 18 thru col. 23 line 29).

As to claims 5 and 16, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the control logic is operable to buffer references to the dirtied blocks of the main memory to be copied (col. 22 line 18 thru col. 23 line 29).

As to claims 6 and 17, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the references to the dirtied blocks comprise addresses for the dirtied blocks (col. 22 line 18 thru col. 23 line 29, bit map reads on this limitation).

As to claims 7 and 18, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein a block of main memory is a page of main memory (col. 22 line 18 thru col. 23 line 29).

As to claims 8 and 19, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein each dirty indicator comprises a single bit (col. 22 line 18 thru col. 23 line 29, bit map).

As to claims 9 and 20, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the direct memory access controller is operable to instigate a search of the dirty memory for dirty indicators indicative of dirtied blocks (col. 22 line 18 thru col. 23 line 29).

As to claim 10, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein each processing set includes a dirty memory (col. 22 line 18 thru col. 23 line 29).

As to claims 11 and 21, Garnet discloses the invention as claimed in the above. Garnet further discloses wherein the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error (Fig. 12 S2).

Response to Arguments

5. Applicant's arguments filed 9/7/04 have been fully considered but they are not persuasive.

In response to applicant's argument on pages 5-7 that the prior arts do not disclose the bridge includes a direct memory access controller that is operable to respond to a fault state by the controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set has been fully considered but it is not persuasive.

Rowlinson discloses the bridge (Fig. 1 Ref, 12 and page 23 middle) includes a direct memory access controller (page 20 bottom, specifically "the operation of the bridge for direct memory access" reads on this limitation) that is operable to respond to a fault state (page 24 lines 5-10, "determined less than the predetermined number of bits" and Fig. 28 Ref S44) by the controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set (abstract and page 23 middle & page 24 lines 5-10).

Alternatively, Garnet the bridge (Fig. 1 Ref, 12 and col. 22 lines 35-49) includes a direct memory access controller (col. 19 lines 37-50 specifically "the operation of the bridge for direct memory access" reads on this limitation) that is operable to respond to a fault state (col. 23 lines 9-11, "determined less than the predetermined number of bits" and Fig. 28 Ref S44) by the controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set (col. 23 lines 12-16).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (571) 272-4180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
November 20, 2004